REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-16 and 32-46 are pending in the application. The Examiner additionally stated that claims 1-46 are rejected. By this amendment, claims 10-14 and 41-45 are cancelled and claims 1-5, 7-9, 15-16, 32-36, 38-39, 40, and 46 are amended. Hence, claims 1-9, 15-16, 32-40, and 46 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §102(e)

The Examiner rejected claims 1-16 and 32-46 under 35 U.S.C. 102(e) as being anticipated by Kyker et al., U.S. Patent No. 6,594,734 (hereinafter, Kyker). Applicant respectfully traverses the Examiner's rejections.

As per claim 1, the Examiner noted that Kyker teaches an apparatus in a pipeline microprocessor (i.e., 301A in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: instruction cache management logic (i.e., 415 in Fig. 4A), configured to receive an address corresponding to a next instruction to be fetched (i.e., the physical address received by the ITLB), and configured to detect that a part of a memory page corresponding to said next instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e., the physical addresses stored in ITLB) and, upon detection, configured to provide said address; and synchronization logic, configured to receive said address from said instruction cache management logic, and configured to direct data cache management logic to check for coherency of the instructions within said

part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction until the stages of the pipeline microprocessor have executed all preceding instructions (e.g., see the abstract, claim 17 and Fig. 4A).

As per claim 32, the Examiner noted that Kyker teaches a method in a pipeline microprocessor (i.e., 301 in Fig. 4A), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: within instruction cache (i.e., 414A in Fig. 4A), detecting that a part of a memory page corresponding to a next instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within the part of the memory page; directing logic within a data cache to check for coherency of the instructions within the part of the memory page; and if the instructions are not coherent, stalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions (e.g., see the abstract, claim 17 and Fig. 4A).

Applicant respectfully disagrees with the Examiner's rejections of claims 1 and 32, along the Examiner's characterization of Kyker. More specifically, it is clear from the recitations of claims 1 and 32 and from the specification that two distinct translation lookaside buffers (TLBs) are claimed: and instruction TLB and an data TLB. Kyker only teaches an ITLB. And although Kyker discloses that his invention is applicable for cache coherency between memory and a cache storing data where a TLB is used, he does not teach a technique that employs both an ITLB and a DTLB each having entries that correspond to an address for a next instruction. Kyker does not suggest or provide any other teaching that would motivate one skilled in the art to provide the apparatus recited in claims 1 and 32, as is argued above. Accordingly, Applicant respectfully requests that the rejections of claims 1 and 32 be withdrawn.

By this amendment, claim 17 has been cancelled, thereby rendering the rejection moot.

Since by this amendment, claims 10-14 and 41-45 have been cancelled, the corresponding rejections are rendered moot.

With respect to claims 2-9 and 15-16, these claims depend from claim 1 and add further limitations over that subject matter which has been argued above to be allowable over Kyker. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 2-9 and 15-16.

With respect to claims 33-40 and 46 these claims depend from claim 32 and add further limitations over that subject matter which has been argued above to be allowable over Kyker. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 33-40 and 46.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1-9, 15-16, 33-40, and 46 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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